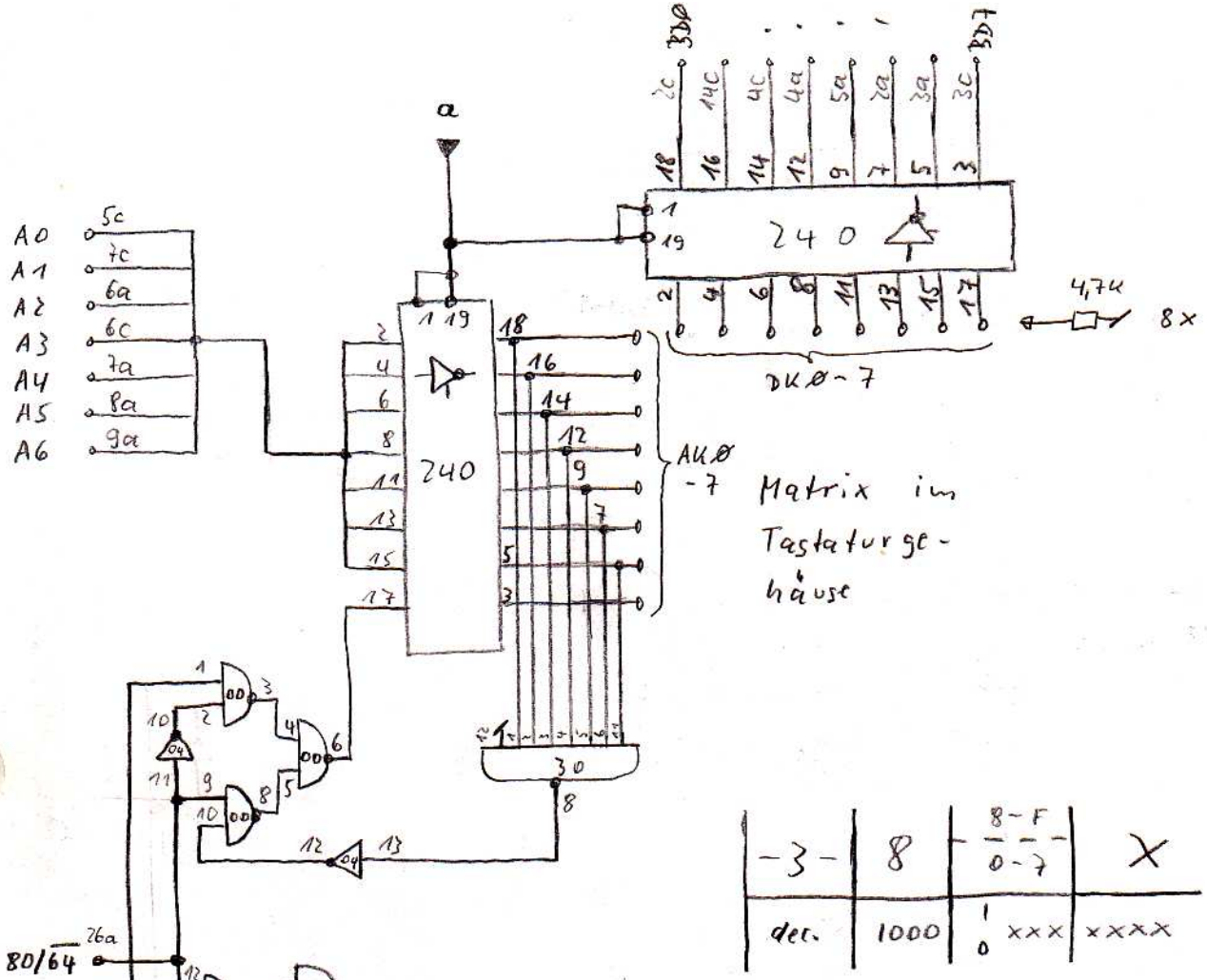
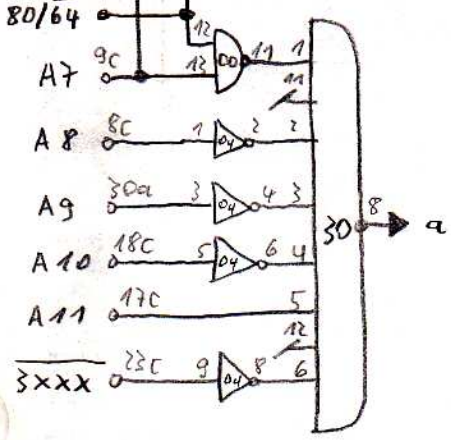
c		a
+5V	1	+5V
DØ	2	D5
D7	3	D6
D2	4	D3
AØ	5	D4
A3	6	A2
A1	7	A4
A8	8	A5
A7	9	A6
	10	$\overline{\text{WAIT}}$
(IEI)	11	$\overline{\text{BUSRQ}}$
(A19)	12	(A18)
HRG	13	+12V
D1	14	RAM1DIS
(-15V)	15	-5V
(IEO)	16	(2PHI)
A11	17	(A17)
A1Ø	18	A14
(A16)	19	+25V ← wird -12V!
$\overline{\text{NMI}}$	20	$\overline{\text{M1}}$
$\overline{\text{INT}}$	21	$\overline{\text{RAM2ENA}}$
$\overline{\text{WR}}$	22	(-12V)
$\overline{\text{3XXX}}$	23	FC
$\overline{\text{RD}}$	24	(Vc MOS)
$\overline{\text{HALT}}$	25	$\overline{\text{Z51}}$
$\overline{\text{BOOT}}$	26	80/$\overline{64}$
A12	27	$\overline{\text{IORQ}}$
A15	28	$\overline{\text{RFSH}}$
PHI	29	A13
$\overline{\text{MREQ}}$	30	A9
$\overline{\text{RESET}}$	31	$\overline{\text{BUSAK}}$
GND	32	GND
c		a

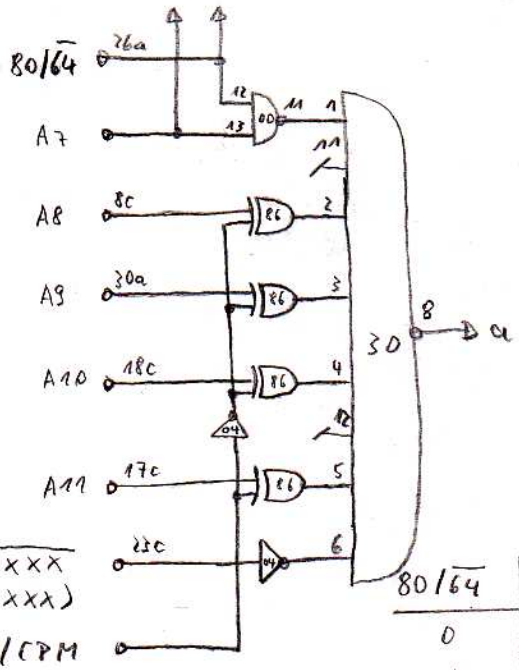


-3-	8	8-F / 0-7	X
dec.	1000	1 / 0 xxx	xxxx



a: $\overline{3800-38FF}$ (64)

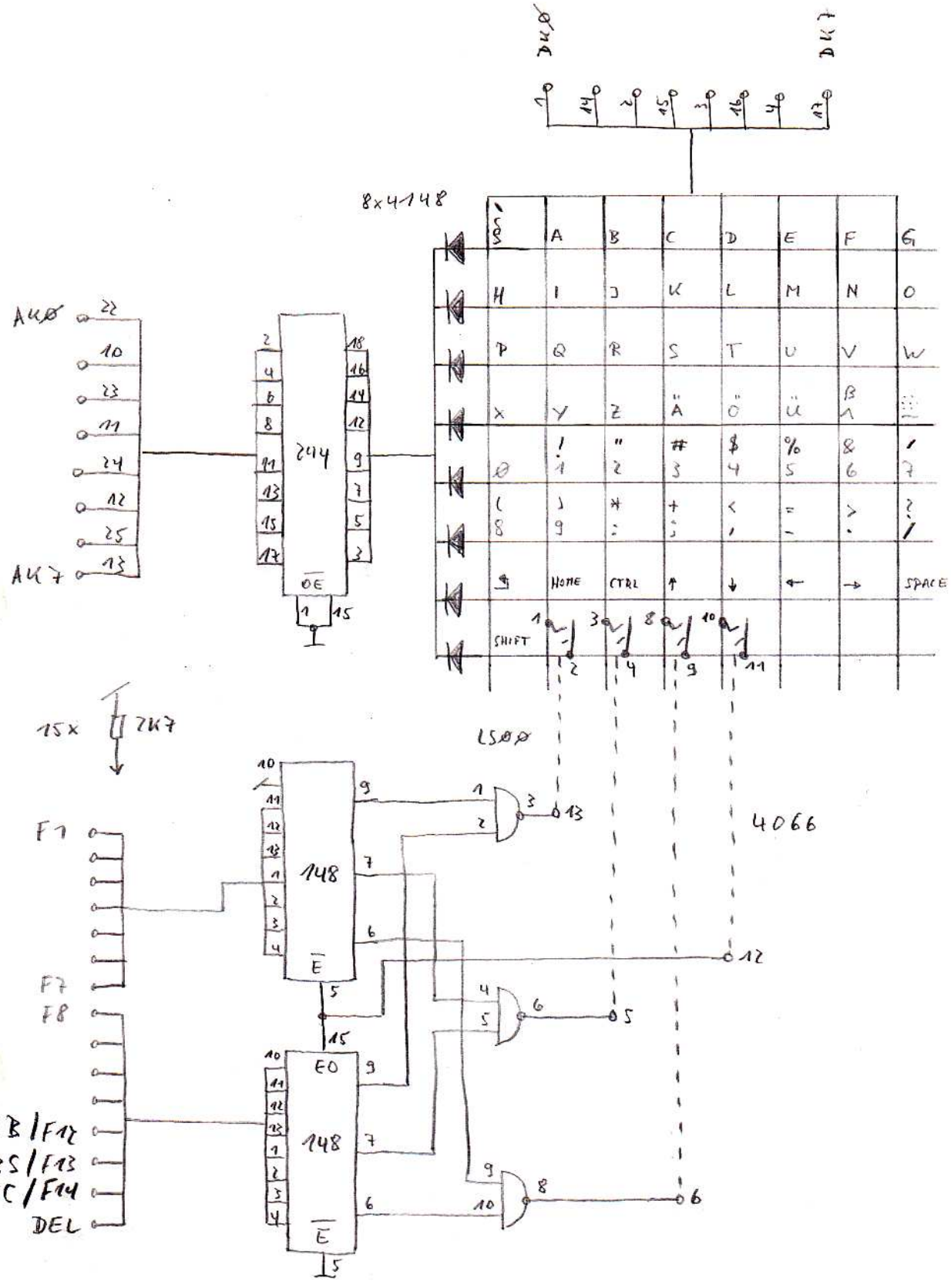
a: $\overline{3800-387F}$ (80)



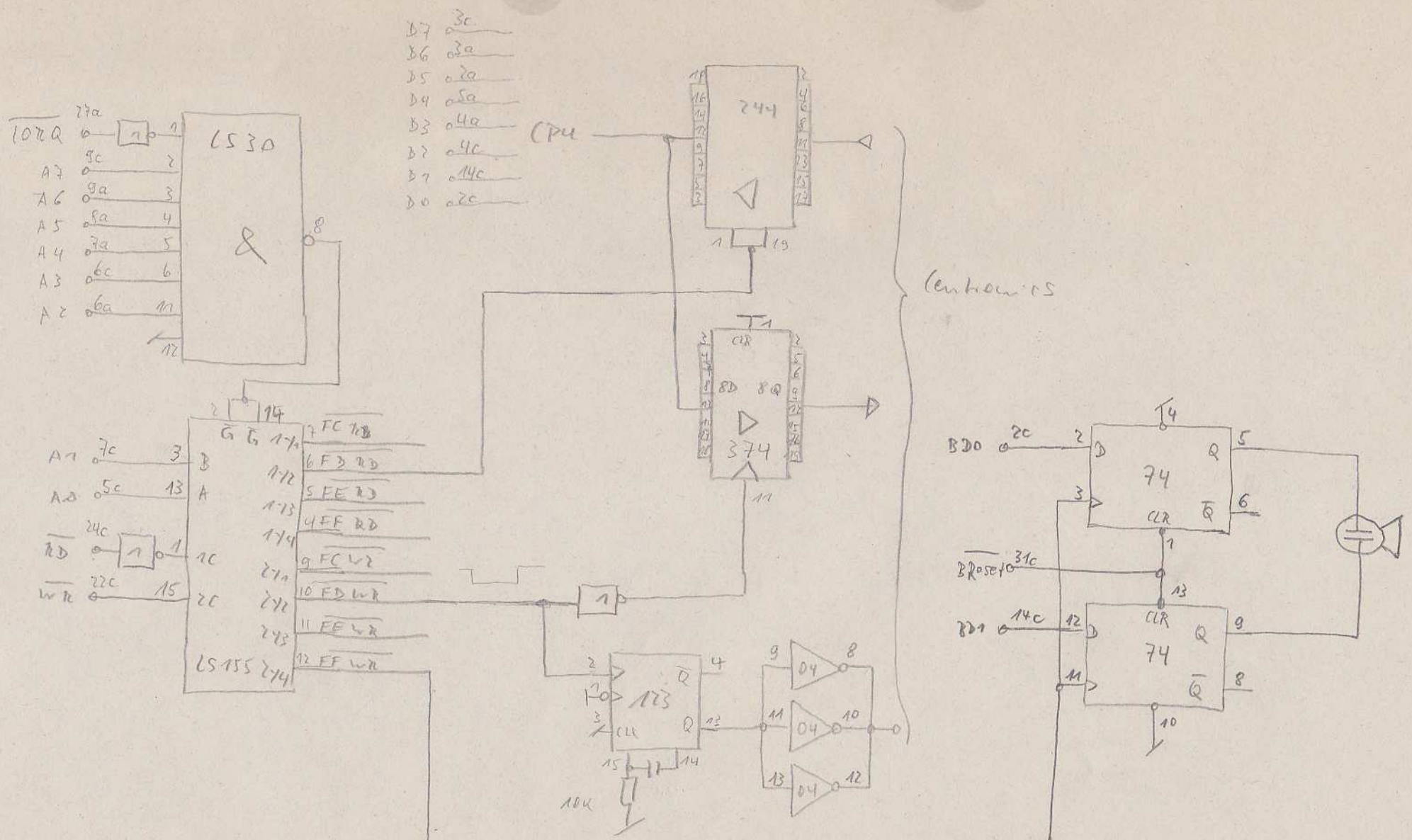
1x 00
1x 04
2x 30
1x 86
2x 240
7

80/64	TRS/CPM	Adressen:
0	0	3800-38FF
1	0	3800-387F
1	1	3700-377F
0	1	3700-37FF x)

x) nicht erlaubt!


DK0
DK7
8x4148
A4Ø
A47
244
ŌE
SHIFT
HOME
CTRL
SPACE
15x 7K7
LSØØ
4066
148
EO
F1
F7
F8
TAB/F12
BS/F13
ESC/F14
DEL

Ä Ö Ü ß BS TAB


D7 3c
D6 3a
D5 2a
D4 5a
D3 4a
D2 4c
D1 14c
D0 2c
CPU
244
LS30
IORQ 17a
A7 9c
A6 9a
A5 8a
A4 7a
A3 6c
A2 6a
374
CLR
8D 8Q
Centronics
LS155
A1 7c
A0 5c
RD 24c
WR 22c
FC WR
FD WR
FE WR
FF WR
173
10K
BDO 2c
BRESET 31c
BD1 14c
74
CLR

Z80B-CPU-Karte mit 64K DRAM

EPROM-KARTE

BA0 … BA11 · BD0 … BD7 · 2732 · 2716 · 241 · 04 · 32 · 08 · 86 · 21 · 30 · 139 · 273 · 244

SRD7 · BRD · SRD5 · SRD4 · SRD3 · SRD2 · SRD1 · SRD0

BA15 · BA14 · BMRQ · BRFSH · BA13 · BA12 · BA11 · BA10 · BA9 · BA8 · BA0-BA6 · BA7

3XXX (FXXX) · 3000-33FF · 3400-37FF · 3800-3FFF (F800-FFFF) · 37XX (F7XX) · 3000-36FF (F000-F6FF) · 3400-36FF · (7F)

BIORQ · BRD · BWR · BRESET · BDO-BD7 · IN · OUT · 7FIN · 7FOUT

RAM2ENA · RAM1DIS

26a	SRD0	64180
25a	SRD1	Z51
13c	SRD2	HGR
23a	SRD3	FC
	SRD4	RAM WRENA (1-3)
	SRD5	RAM SEL 2
	SRD6	TRS/CPM
	SRD7	ROM DIS 1-4

4 × EPROM
1 × 139
5 × 32
2 × 04
1 × 08
1 × 21
2 × 30
1 × 241
1 × 244
1 × 273

VDU-Karte

Clock Select:
L: 3900 - 3FFF (11)
H: 3880 - 3FFF (14)

Clock Select ← 26a ○ 80/64
CHR Select ← 25a ○ Z51

1 x 00
3 x 04
1 x 08
1 x 10
1 x 27
1 x 30
2 x 32
1 x 74
1 x 93
1 x 122
3 x 157
1 x 166
2 x 245
1 x 374
2 x 6116
2 x 2732
1 x 6845

2x BC109C

*) vorerst durch 74LS32 ersetzt
später 74LS86!

BD Ø
BD 7
BA Ø
BA 1
BINT
BA 11
BA 4
3XXX
BA 3
BA 2
BWR
BRD
BReset

367
174
123
74
4518
155
2793
90
93

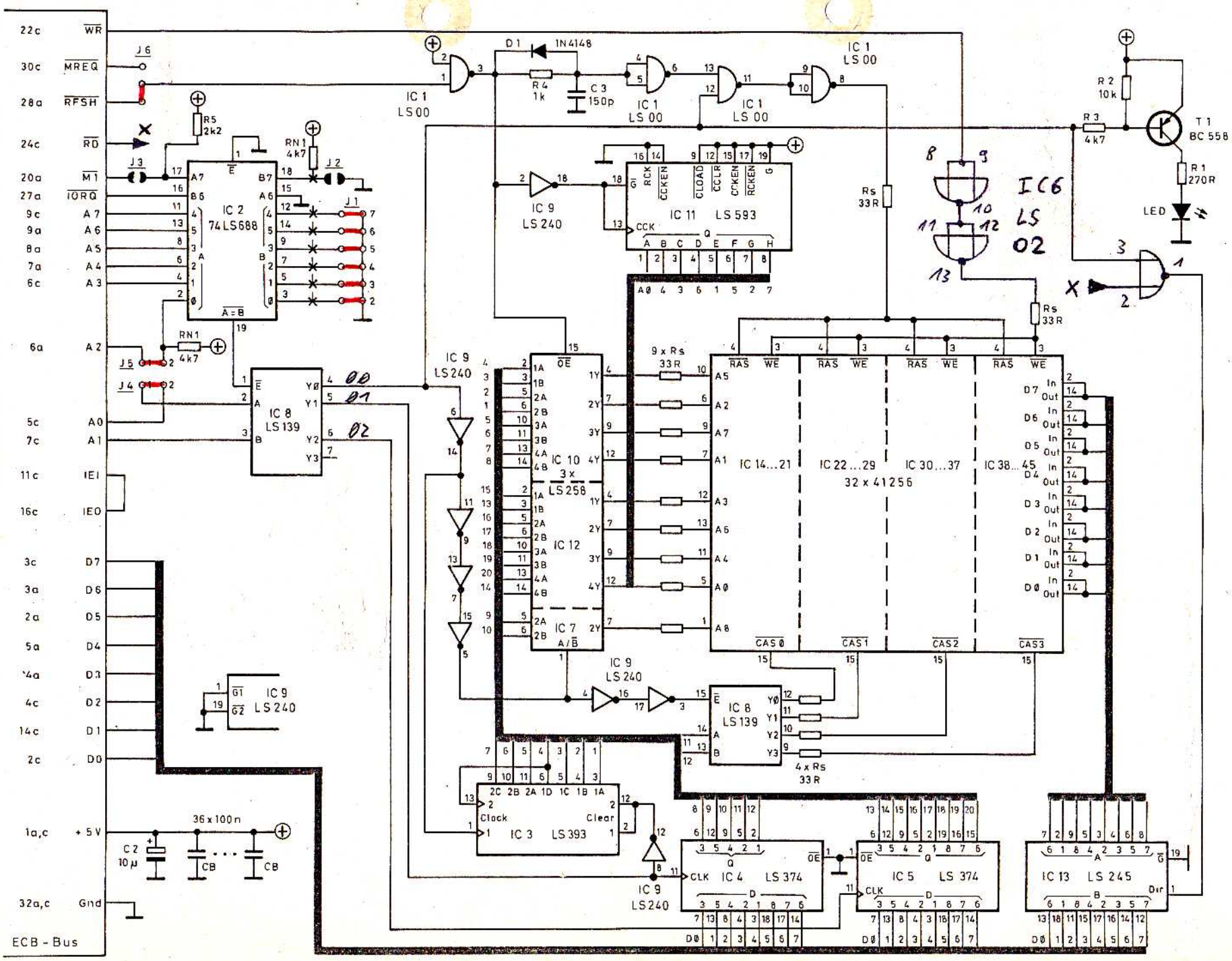
DS Ø
DS 1
DS 2
SIDE SELECT
MOTOR ON
WRITE GATE
WRITE DATA
DIRECTION
STEP
HEAD LOAD
READY
INDEX
WRITE PROTECT
TRACK Ø
RAW READ

Jumper:

34 pol.

Floppy-Controller

SD + DD 5 1/4 2011



00: DATA-PORT 01: Sector-Port 02: Track-Port